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MCQs Digital Logic Design. 1. When we input two values 0 and 1 which of the following gates would output 1? A. OR gate B. NAND gate C. AND gate D. both a and c

MCQs Digital Logic Design | T4Tutorials

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(PDF) Digital Logic Design - ResearchGate

5 Volt series, if certain voltage is applied on the input, the output voltage of Logic high signal (V_{OH}) will be in the range of _____ volts. 4 to 4.5 4.5 to 5 0 to 4.5 0 to 3.5 18. $A.(B.C) = (A.B).C$ is an expression of _____ Demorgan's Law Distributive Law Commutative Law Associative Law (Page 72) 19.

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“Combinational logic circuits” “Sequential logic circuits” “How digital logic gates are built using transistors” “Design and build of digital logic systems. Course Structure 11 Lectures ...” J. P. Hayes, “Introduction to Digital Logic Design,” Addison-Wesley, 1993.

Digital Electronics Part I “Combinational and Sequential

Digital Logic Design: Home Page : Mcqs : Video ... The divide-by-60 counter in digital clock is implemented by using two cascading counters ... Mod-50, Mod-6: A: 4: In NOR gate based S-R latch if both S and R inputs are set to logic 0, the previous output state is maintained: True: False : A: 5: The minimum time for which the input signal has ...

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Next Page Previous Page Multiple choice Questions Digital Logic Design 1. How many bits must each word have in one-to-four line de-multiplexer to be implemented using a memory? A. 8 bit B. 4 bits C.

Multiple choice Questions Digital Logic Design | T4Tutorials

Multiple Choice Questions and Answers on Digital Electronics . Objective Questions and Answers on Digital Electronics Explanation: Since $V(1)$ is lower state than $V(0)$ it is a negative logic circuit. Since diodes are in parallel, it is an OR gate. Q24.

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Digital Logic Design - unipi.it

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than 100 but less than 9999 d. More than 100 but less than 999 2. Typical size of digital IC chip is a. "1Å—1" " b. "2Å—2 " c. 0.1Å—0.1" d. 0.001"Å—0.001 3. IC chip used in digital clock is a. SSI b. LSI c. VLSI d. MSI 4.

Logic Families - gatestudy.com

COE/EE 243 Digital Logic Session 44; Page 1/5 Spring 2003 COE/EE 243 Sample Final Exam From Fall 98 Solutions Show your work. Do NOT use a calculator! 1. (9 pts) Complete the following table of equivalent values.

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Digital Logic Design BiBasics Combinational Circuits Sequential Circuits Pu-Jen Cheng Adapted from the slides prepared by S. Dandamudi for the book, Fundamentals of Computer Organization and Design.

Digital Logic Design - âœƒ««è†°ç•£âª§â-,

questions in 10 seconds like some university multiple choice questions. Some questions may have ... Q. Design a digital circuit to delay the negative edge of the input ... The digital circuit is shown with logic delay (dly3) and two clock buffer delays (dly1, dly2).

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DigitalLogic - Computer Science

RAM & ROM Based Digital Design ECE 152A â€“ Winter 2012. March 12, 2012 ECE 152A - Digital Design

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What Is Digital Logic Design? - Learn.org

CS302 Solved Quiz 1 " MCQs " Digital Logic Design FALL 2011. Shared by Tariq Aziz (Alone Magic) www.vuzs.info Question 1. A standard SOP form has _____ terms that have all the variables in the domain of the expression.

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Basics of Digital Logic Design - Computer Science and

Name: _____ Student ID: _____ Computer Architecture I: Digital Logic 03-60265 Summer 2005 Instructor: Dr. Y. M. Alginahi Date: June 14, 2005 Section 1 /30 ... 5- For the multiple choice questions, there is only one correct answer so make sure to mark only one answer. If more than one answer is checked then no marks will be

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